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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,509	07/16/2004	Gaurav Kumar VARSHNEY	TI-38654	4508

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,509	VARSHNEY ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above claim(s) *21-44 and 65-88* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 45-47* is/are rejected.

7)☒ Claim(s) *4-20 and 48-64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 07/16/2004. **Claims 1-88** are pending.

Election/Restrictions

1. This application contains claim groups directed to the following patentably distinct species of the claimed invention:

I **(Claims 1-20 and 45-64)** drawn to a method of reducing computational resource in characterizing a parameter for a combination of an input pin and output pin of a cell with determining a worst case vector.

II. **(Claims 21-29, 41-44, 65-73, and 85-88)** drawn to a method of reducing computational resource in characterizing a noise immunity for a combination of an input pin and output pin of a cell.

III. **(Claims 35-39 and 79-83)** drawn to a method of reducing computational resource with characterizing a noise immunity for a combination of an input pin and output pin of a sequential element with applying input transition waveform.

IV. **(Claims 30-34 and 74-78)** drawn to a method of reducing computational resource in characterizing a noise propagation (NP) parameter.

V. **(Claims 40 and 84)** drawn to a method of reducing computational resource in characterizing a noise immunity parameter and a noise propagation parameter with determining a first start NP curve and a second start NP curve.

2. During a telephone conversation with Alan Stewart (Reg. No. 35,373) on 07/11/2006, a provisional election was made **without traverse** to prosecute the

invention of **group I (claims 1-20 and 45-64).** Affirmation of this election must be made by applicant in replying to this Office action. **Claims 21- 44 and 65-88** are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1 and 45 are rejected** under 35 U.S.C. § **102(e)** as being anticipated by **Elzingga** (US Parent Pub. No. 2003/0115557).

(Claim 1 and similarly recited claim 45)

A method / a computer readable medium of reducing computational resources in characterizing a parameter for a combination of an input pin and an output pin of a cell, said cell being contained in a library used in the design of an integrated circuit, said method comprises:

determining a worst case vector, wherein said worst case vector represents a set of input bits, with each of said input bits being applied to a corresponding one of a set of input pins other than said input pin of said combination, wherein said worst case vector would cause propagation of most noise from said input pin to said output pin among vectors which would cause a bit value transition on said output pin if the input bit value is changed on said input pin (Elzinga; abstract; Figs. 2 and 3; paragraphs[0005] and [0035]-0047]); and

computing a plurality of data values for said parameter when said worst case vector is applied to said set of input pins, wherein said plurality of data values are used in an analysis of said integrated circuit irrespective of which of said vectors is applied to said set of input pins (Elzinga; abstract; Figs. 2 and 3; paragraphs[0005] and [0035]-0047]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 2-3 and 46-47** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Elzingga** in view of **Wu et al.** (US Patent No. 2004/0015339).

(Claim 2 and similarly recited claim 46)

Elzingga disclose the method/ the computer readable medium of claim 1/claim 45 respectively, **except** wherein said determining comprises:

applying a plurality of glitches to said cell for each of said vectors; and

examining an output glitch corresponding to each of said plurality of glitches on said output pin to determine said worst case vector.

Wu et al. disclose wherein said determining comprises:

applying a plurality of glitches to said cell for each of said vectors (Wu et al.; abstract; Figs. 2 and 4; paragraphs[0021]-[0022]); and

examining an output glitch corresponding to each of said plurality of glitches on said output pin to determine said worst case vector (Wu et al.; abstract; Figs. 2 , 4-5, and 6; paragraphs[0021]-[0034]; paragraphs[0038]-[0040]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Elzingga with the teaching of Wu et al. because using glitch to determine worst case vector would provide a more accurate in the treatment of noise propagation and its effect on subsequence cells (Wu et al.; paragraph [0021])

(Claim 3 and similarly recited claim 47)

The method/ the computer readable medium of claim 2/ claim 46 respectively, wherein all of said plurality of glitches have the same width and each of said plurality of input glitches has a different height, and wherein said examining examines a height

corresponding to each of said output glitches on said output pin (Wu et al.; abstract; Figs. 2 and 4; paragraphs [0021]-[0022]).

Allowable Subject Matter

8. **Claims 4-20 and 48-64** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. **Claims 4-5** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 4)

wherein said applying and said examining determine at least three immunity transition points for each of said vectors, wherein each of said immunity transition points indicates a minimum height of said plurality of glitches at which the height of said output glitch exceeds a first threshold, said method comprises: plotting a curve corresponding to each of said vectors based on said at least three immunity transition points, wherein a vector corresponding to the curve with the least heights is determined to be said worst case vector.

10. **Claims 6-18** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 6)

wherein said parameter comprises noise immunity, wherein a failure result is deemed to be obtained for an input glitch of a first height and a first width if the height of an output glitch corresponding to said input glitch exceeds a first threshold voltage, and

a success result is deemed to be obtained otherwise, said method further comprises generating a noise immunity curve (NIC) corresponding to only said worst case vector, wherein said NIC contains a plurality of immunity transition points, wherein each of said plurality of immunity transition points indicates a minimum value for one dimension of said input glitch required for said failure result for each of a value of the other dimension.

11. **Claims 19-20** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 19)

wherein said cell comprises a sequential element, said method further comprising: applying an input transition waveform having a height equaling the height of an input glitch of interest, said input transition waveform being associated with reference to a clock signal to provide infinite setup and hold times for said sequential element to latch said input transition waveform; examining the output signal generated by said sequential element to determine whether sufficient noise was propagated by said sequential element; and determining that sweep can be avoided for all widths of the input glitches of said height if sufficient noise is not propagated by said sequential element.

12. **Claims 48-49** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 48)

wherein said applying and said examining determine at least three immunity transition points for each of said vectors, wherein each of said immunity transition points indicates a minimum height of said plurality of glitches at which the height of said output glitch exceeds a first threshold, said method comprises: plotting a curve corresponding to each of said vectors based on said at least three immunity transition points, wherein a vector corresponding to the curve with the least heights is determined to be said worst case vector.

13. **Claims 50-62** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 50)

wherein said parameter comprises noise immunity, wherein a failure result is deemed to be obtained for an input glitch of a first height and a first width if the height of an output glitch corresponding to said input glitch exceeds a first threshold voltage, and a success result is deemed to be obtained otherwise, said method further comprises generating a noise immunity curve (NIC) corresponding to only said worst case vector, wherein said NIC contains a plurality of immunity transition points, wherein each of said plurality of immunity transition points indicates a minimum value for one dimension of said input glitch required for said failure result for each of a value of the other dimension.

14. **Claims 63-64** would be allowable because the prior art of record does not teach or fairly suggest the limitations in:

(Claim 63)

wherein said cell comprises a sequential element, further comprising: applying an input transition waveform having a height equaling the height of an input glitch of interest, said input transition waveform being associated with reference to a clock signal to provide infinite setup and hold times for said sequential element to latch said input transition waveform; examining the output signal generated by said sequential element to determine whether sufficient noise was propagated by said sequential element; and determining that sweep can be avoided for all widths of the input glitches of said height if sufficient noise is not propagated by said sequential element.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Patent Examiner
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PRIMARY EXAMINER